CONTROLLING OF RANGE-GATED MTI RADAR WITH DIGITAL TECHNIQUES

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THESIS

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With Digital Techniques

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June 1971

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Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
June 1971

ABSTRACT

The timing and gating circuitry necessary for twenty channels of range-gated MTI radar was constructed. By the incorporation of a variable delay in the commencement of the range-gate sampling interval it was possible to extend the effective range over which the gates operated. The use of digital techniques with integrated circuits provided a means by which the twenty channels may easily be extended to any number required for a particular radar application. Performance of the circuitry was demonstrated in conjunction with a typical channel of range-gated MTI radar.

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I. INTRODUCTION

The Moving-Target Indicator (MTI) radar is a pulsed radar system in which the doppler frequency shift of moving tragets is used to distinguish them from fixed targets. By employing a pulsed radar instead of continuous wave, moving targets can be detected in the presence of echos from stationary objects having a return on the order of 30 dB greater than that of the moving target.

Any object moving with a radial velocity relative to that of the radar will present a frequency shift in the reflected signal given by:

$$f_d = \frac{103\ v_r}{\lambda}$$

where: f_d = doppler frequency in Hertz

v_r = relative radial velocity in knots

λ = wavelength of radar in cm.

The undesired returns such as those from terrain, vegatation, weather, and sea waves are termed clutter since they clutter a PPI scope. By their very nature they tend to have low doppler frequencies, so by removing echos with little or no frequency shift it is possible to eliminate much of the clutter.

Skolnik [Reference 1] indicates the return echo from a target can be represented by:

$$V = K \sin \left[2\pi\ (f_c + f_d)\ t - \frac{4\pi f_c\ R}{c}\right]$$

where: K = amplitude of a signal from a target at range R

f_c = radar carrier frequency

f_d = target doppler shift

c = velocity of propagation

R = initial range to target.

If the return echo and a reference signal are mixed in a coherent detector and the difference frequency is extracted:

$$V_{diff} = K \sin \left(2\pi f_d t - \frac{4\pi f_c R}{c}\right)$$

Thus it is seen that the difference frequency is f_c and that for stationary targets V_{diff} will take on a constant dc value between $\pm$ K. Other clutter normally has a lower relative velocity and the resulting small doppler shift produces only slight variations away from the dc value.

It would appear that a high-pass filter would eliminate the clutter, but the problem is not quite so simple. In the first place antenna rotation introduces modulation on all returns. Recent work [Ref. 2] indicates that some clutter produces doppler returns which are higher in frequency than expected. A third complicating factor is that the frequency spectrum of the typical pulsed radar exhibits a sin x/x characteristic about f_c with spectral lines reflected at the carrier frequency with additional lines separated by multiples of the pulse repetition frequency. Target and clutter echos are associated with each of these lines. Thus a comb filter of the type described by Washam [Ref. 3] is required to obtain high clutter rejection.

The maximum velocity of moving clutter, and hence the bandwidth of clutter spectrum, is a function of the radar environment. A desirable feature of the radar is that the lower cut-off frequency of the comb filter be variable so that it is operator-adjustable as clutter conditions dictate.

In general there are two means by which MTI radar obtains the desired comb-filter characteristic. The first and to date most widely used method is the delay-line canceler. The second uses range gates. Until recently this second method has been too complicated and expensive to be in general use. The introduction of intergrated-circuit technology has made it more attractive, however, and several systems have been built.

As essential feature of range-gated MTI radar is the timing and gating circuitry. The growing number of logical functions which can be placed on one integrated circuit makes digital control of these timing and gating functions an attractive prospect as far as cost, weight reduction, and complexity of range-gated MTI is concerned.

II. GENERAL DISCUSSION OF MTI

A. DELAY-LINE CANCELER

Successive echo pulses from stationary targets are separated in time by the pulse repetition period of the particular radar in use, and the successive detected pulses are nearly equal in amplitude. Thus, if two successive pulse trains are subtracted, the fixed-target clutter is eliminated and that which remains is the moving-target intelligence. This filtering in the time domain is the function of the delay-line canceler, which to this time has been the primary technique used in MTI radar. It is accomplished by providing two paths for the return echo as can be seen in the simplified block diagram of Figure 1.

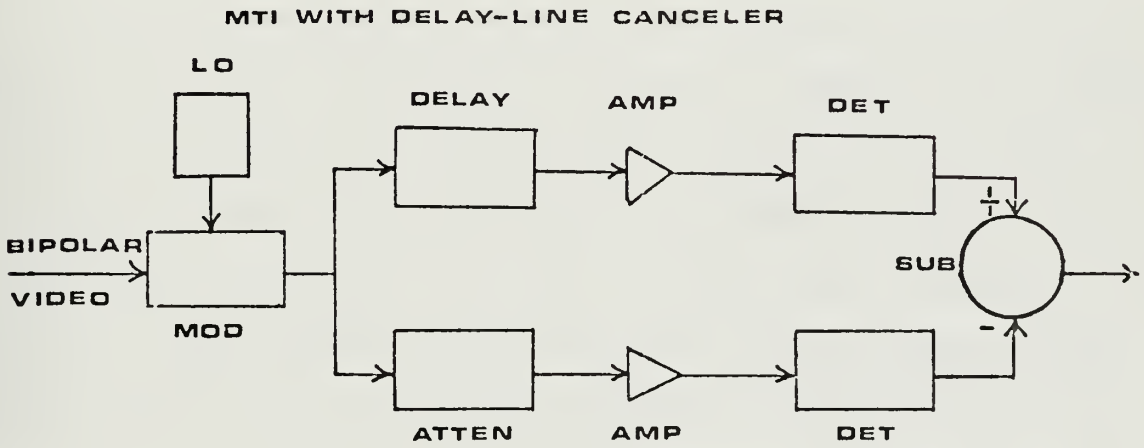


FIGURE 1

Since the delay introduced in one path is the reciprocal of the pulse repetition frequency, the signal appearing at the output of the subtractor is the difference of two successive pulse trains. The single delay-line canceler does not have the characteristics of the ideal comb filter required. According to Skolnik [Ref. 1] its frequency response

characteristic is represented by Figure 2 and is given by V = K sin (π f_d = T).

FREQUENCY RESPONSE OF SINGLE DELAY-LINE CANCELER

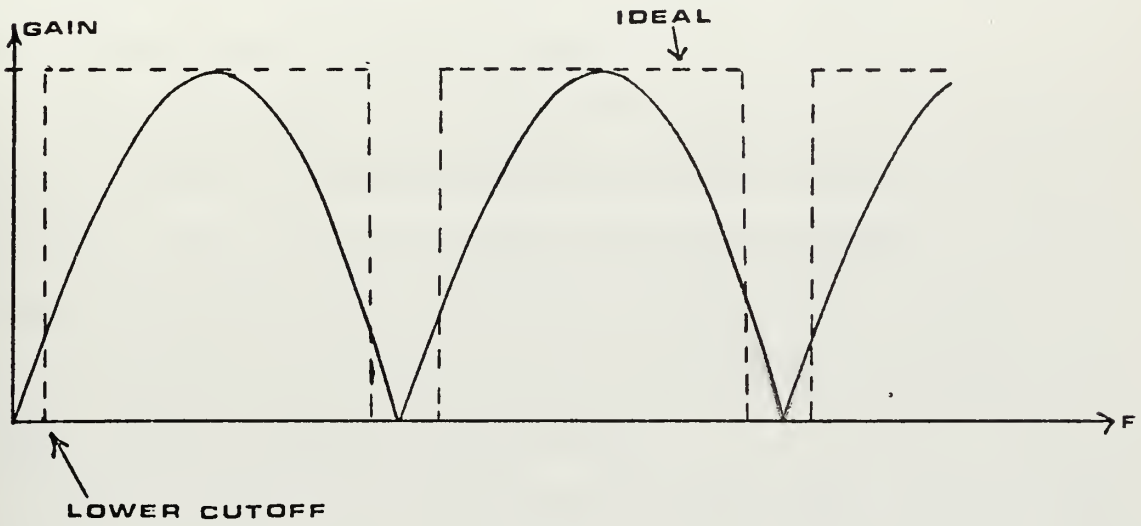


FIGURE 2

When the target doppler frequency is any integral multiple of the PRF (f_d = n/T = nf_r) cancellation occurs and that target is lost. The speed which produces such a doppler shift is known as a blind speed.

Most MTI radars have a pulse repetition frequency (PRF) less than 1000 Hz; thus delay times on the order of a millisecond or more are required. Electromagnetic delay lines can not readily produce delays of this magnitude. It is therefore convenient to change the electromagnetic energy to acoustic energy which propagates at a much slower rate. The medium of propagation is usually mercury contained in a cylindrical tube or quartz in the form of a many faceted fused block though other media have been used. Almost all schemes use a piezoelectric transducer at each end of the delay line. It is necessary to place the signal on a high-frequency carrier because of the band-pass characteristic of the transducer.

One disadvantage of the delay-line canceler is that the insertion loss of the delay line can be as much as 70 dB, so an amplifier is required at the output. Since this amplifier can produce undesired phase changes in the signal, a similar amplifier is usually placed in the undelayed branch to maintain coherency.

Other disadvantages of the delay-line canceler are that the line itself is temperature dependent and that spurious signals may arise in the medium. The system has stringent tolerance requirements in the two channels if degradation in cancellation is not to occur. Although there are two parallel channels in the system, if any element in either channel fails the system as a whole fails.

Once the delay line is constructed the delay time is fixed. This fixes the PRF of the radar. Therefore, it is not possible to use a variable PRF to eliminate blind speeds without utilizing complicated switching techniques to change delay times as required. Despite these problems the single delay-line canceler has been the mainstay of MTI radar. Clutter cancellation on the order of 40 dB can be realized with a single delay line and improved filter response characteristics can be obtained when multiple delay lines are used in appropriate configurations. These are discussed as some length by White and Steinberg [Refs. 4 and 5].

B. RANGE-GATED MTI

Since the doppler frequencies are relatively low, a low-frequency band-pass filter with upper cutoff frequency less than the pulse repetition frequency might be used to pass the doppler information. This filter, however, has two serious limitations when applied to the MTI system. First, the nature of the narrow-band filter destroys the range information contained in the echo. Second, the signal-to-noise ratio

is degraded because of the collapsing loss caused by noise entering the filter from ranges not containing target information. These limitations can be overcome by quantizing the bipolar video in range gates and processing the data in multiple parallel channels. Range and range resolution are now obtained from the range gates since any particular channel will process only target information, noise, and clutter contained in a short time interval. The collapsing loss is eliminated because noise from other ranges can not enter a given range gate.

The filter which will reject clutter frequencies and pass the target information is a matched notch filter which maximizes the signal-to-clutter ratio and is depicted as the ideal filter in Figure 2. While it can be approximated in the time domain by employing multiple delays, this is a difficult technique to put into practice.

If a band-pass filter follows each range gate, the range and doppler information contained in the signal is not lost. Range resolution of the radar will be limited by the duration of the range gate, the pulse width, the system bandwidth, or a combination of these.

While this method still is subject to blind speeds at $f_d = nf_r$, multiple pulse repetition frequencies can be utilized quite easily to reduce the problem. A further advantage of this scheme over the delay-line canceler is that with the multiple parallel channels the failure of one channel will not cause a failure of the entire system.

It has been the size, weight complexity and cost of the multiple-channel technique which, until the advent of the large scale integration (LSI), has precluded wide-spread use of range-gate MTI except for special applications. Several range-gated MTI radars have been built, tested and reported in recent years [Refs. 6, 7, and 8] and of special interest is the single channel tested and reported by Washam [Ref. 3].

One form of the multichannel range-gated MTI radar is represented in block diagram form in Figure 3.

RANGE-GATED MTI

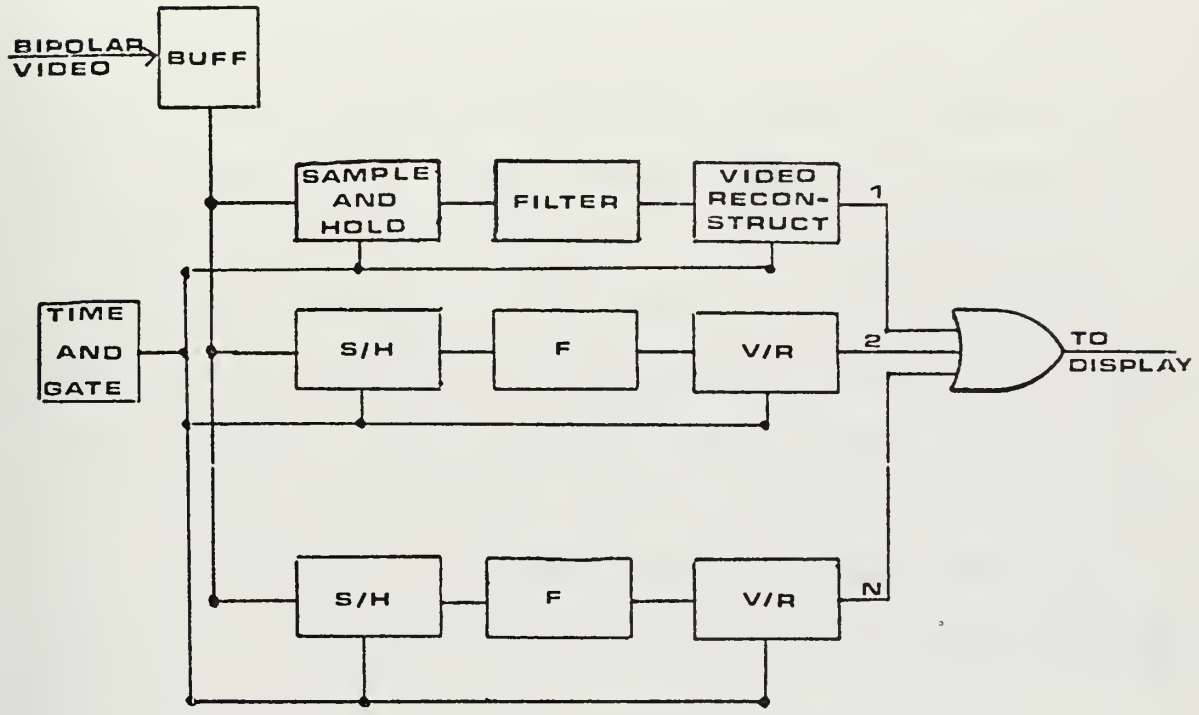


FIGURE 3 (AFTER HOISINGTON)

In a range-gated MTI the radar return is passed through RF, IF, and detection stages as if a delay-line canceler were to be used. The resulting bipolar video is then presented at the input of each of the n channels. At the time corresponding to a given range as determined by the gating and timing circuitry, a sample of the video is placed and stored on the appropriate holding capacitor until the completion of one repetition period. Following the next transmitted pulse a new sample is taken. If the input to the sample-and-hold circuit is a signal of constant amplitude and any multiple of the sampling frequency, the output will appear as a constant dc value. Since the doppler filter removes dc

and low frequencies, all zero doppler returns and all blind speed returns will be eliminated. Another characteristic of the sample-and-hold circuit is that no matter what the doppler frequency, the maximum output frequency of the sample-and-hold circuit will be one half the sampling frequency. Thus the limits of the doppler filter passband are set between the clutter cut off (variable) and one half the sampling frequency. This can be shown by the sampling theorem of Shannon which states in essence that the highest frequency which can be obtained from a sampled wave form is that which is one half of the sampling frequency.

The output of the doppler filter passes to the video reconstruct circuit where it is rectified and integrated by a low-pass filter having a long time constant. The gating pulse, which is common to the sample and hold and the video reconstruct circuitry, permits the signal to pass to a buss common to all of the range channels. The video signal, now reconstructed, is directed to the appropriate display or data-processing device from this buss.

It is obvious that the longer the range of the radar, the more channels will be required to cover that range for any given width of the sample gate. For instance, an AN/UPS-1 has a pulse width of 1.4 usec. If the sample gate used has a width of 2 usec the range resolution will be limited to not less than 300 meters. Thus for a radar range of 80 nautical miles, 495 channels would be required to give MTI operation to maximum range. This requirement is modified by the fact that beyond a certain range fixed clutter may no longer be a problem, and normal video techniques can be used.

Though the isolated nature of clutter return in many cases reduces the total number of required channels for effective range-gated MTI, a nontrivial number remain. It would be useful to be able to test a

limited number of channels over the range of the radar before constructing the entire system. To accomplish this objective timing and gating circuitry is required to place and operate the limited number of channels in a desired range window. The realization of such circuitry is discussed in the next section.

III. EXPERIMENTAL PROCEDURE

The objective of this work was to provide the circuitry necessary for the timing and gating of n channels of a range-gated MTI radar. Because of the impractibility of constructing all of the channels required for the full range of the radar, the project was split into two parts.

The first step was to provide, after the radar synchronizing pulse, a variable delay before the first range gate is enabled. This delay varies from zero to 200 usec, can be preset by the operator, and has the effect of moving the range interval that can be processed from zero to about 16 nmi.

The second requirement was to provide the gating pulses for twenty successive range channels. The design was to be such that the resulting hardware can easily be extended to include additional channels. It is anticipated that testing and evaluation will be performed in conjunction with the AN/UPS-1 radar which has a pulse repetition frequency of 800 Hz and a pulse width of 1.4 usec. In most applications the sampling frequency is approximately the reciprocal of the pulse width. For evaluating the optimum sampling frequency to use with the AN/UPS-1 a variable sampling frequency from 0.5 to 2.0 MHz was provided.

A. GENERAL DESIGN CONSIDERATIONS

To be competitive in size, weight and cost with the delay-line technique, a range-gated MTI must make use of recent advances in integrated circuit technology. For this reason an early decision was made to realize the timing circuits with integrated circuits using digital

techniques. To make use of existing and available range channels the design provided for mounting the hardware on printed-circuit boards which are compatable with the existing circuits.

The relatively rapid clock rate of 4 MHz and the fast rise time necessary to ensure that the range gate was enabled for the entire gate width made the selection of transistor-transistor logic (T^2L) devices as the basic building blocks an obvious choice. The use of DTL (diode-transistor logic) buffers which have the advantage of a higher fanout capability than the T^2L was possible at certain points.

A general description of the delay and gating circuits can be followed by reference to the block diagram in Figure 4. The use of digital techniques requires that the delay be quantized and it was decided to provide delay from zero to 200 usec in steps of 2 usec.

This step size was realized by an appropriate division of the basic clock rate while synchronization of the timing circuitry was provided by the trigger pulse of the AN/UPS-1 radar. This pulse toggled a flip-flop from the low state to the high state. The high output (Q) of the flip-flop was logically ANDed with the output of the dividing circuitry which permitted a 0.5 MHz pulse train to be applied to a decimal counter in synchronization with the radar pulse. The counter was decoded at each clock pulse.

The counter/decoder was configured such that a high level appeared at its output and counting stopped when the preselected count (delay) was reached. This high level was logically ANDed with the basic clock enabling the clock pulses to toggle a second counter/decoder. From this device every count was decoded and used to produce the range gate pulses. After completing the count for n channels one of the succeeding count pulses was used to reset the counters and flip-flop for the next cycle.

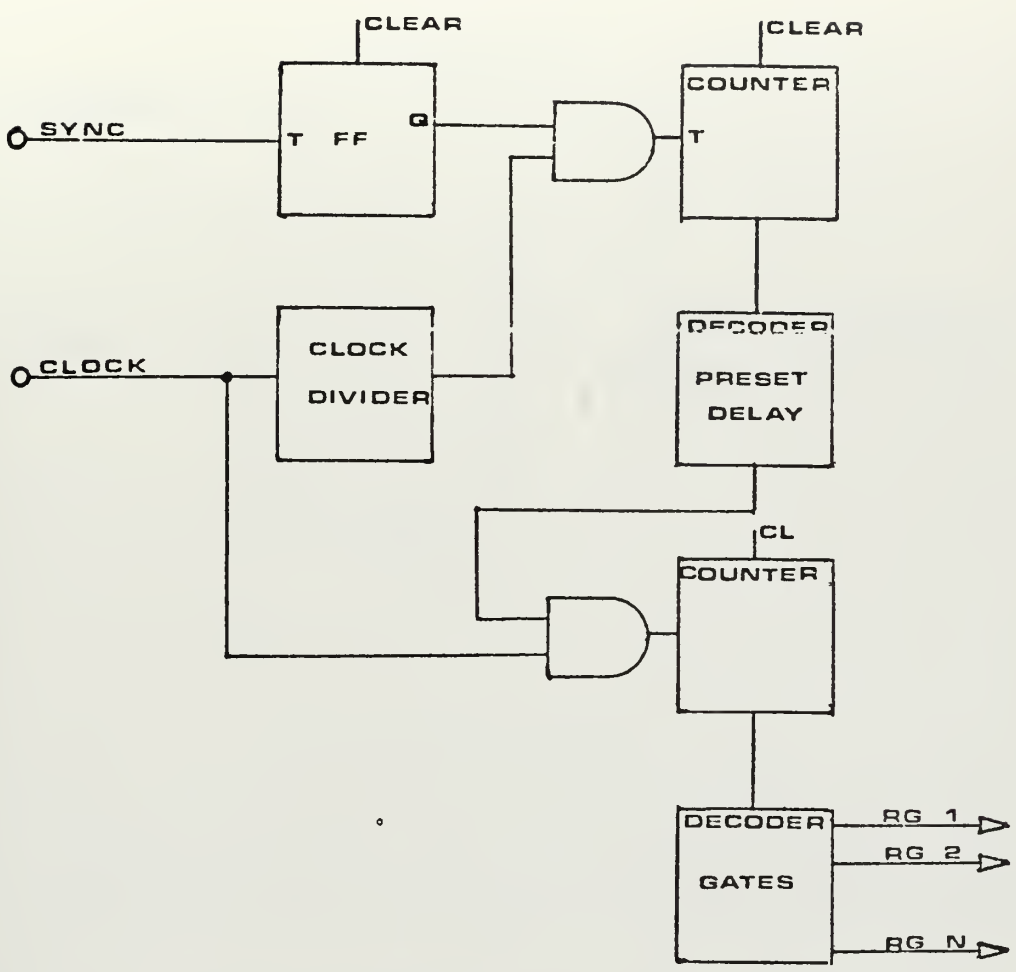


FIGURE 4

B. CLOCK DIVIDING

In order to produce the 0.5 MHz clock for the 2 usec step delay it was necessary to provide a switched dividing circuit as in Figure 5. The assumption was made that the basic clock rate would be 0.5, 1.0, 2.0 or 4.0 MHz.

The divide-by-eight and divide-by-four circuits were constructed from Fairchild 9300 four-bit shift registers from the divide-by-n counter of Figure 9, pg.3-26 of Ref. 9 . The divide-by-two circuit was realized by using one half of a single Fairchild 9020 JK flip-flop configured as a T flip-flop. The resulting output is shown in idealized form in Figure 6.

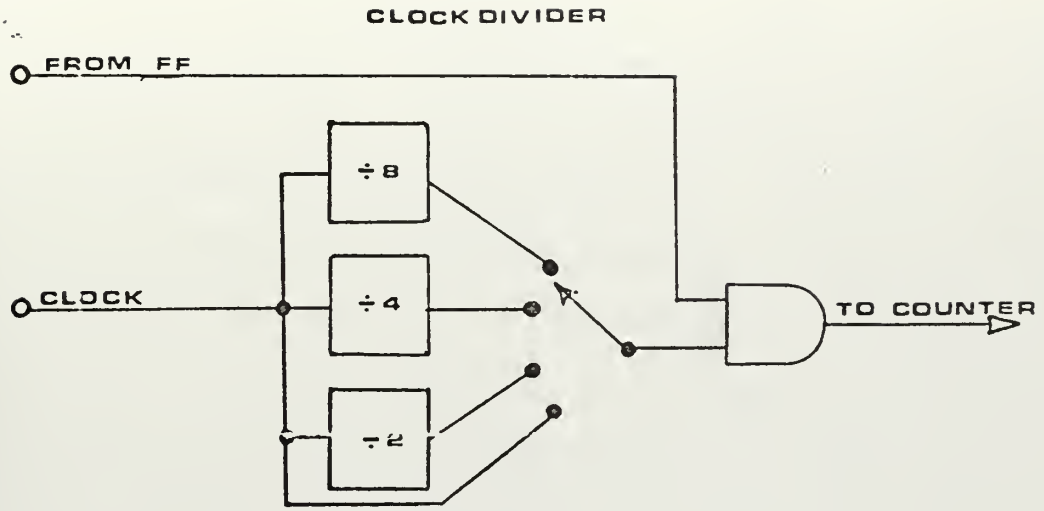


FIGURE 5

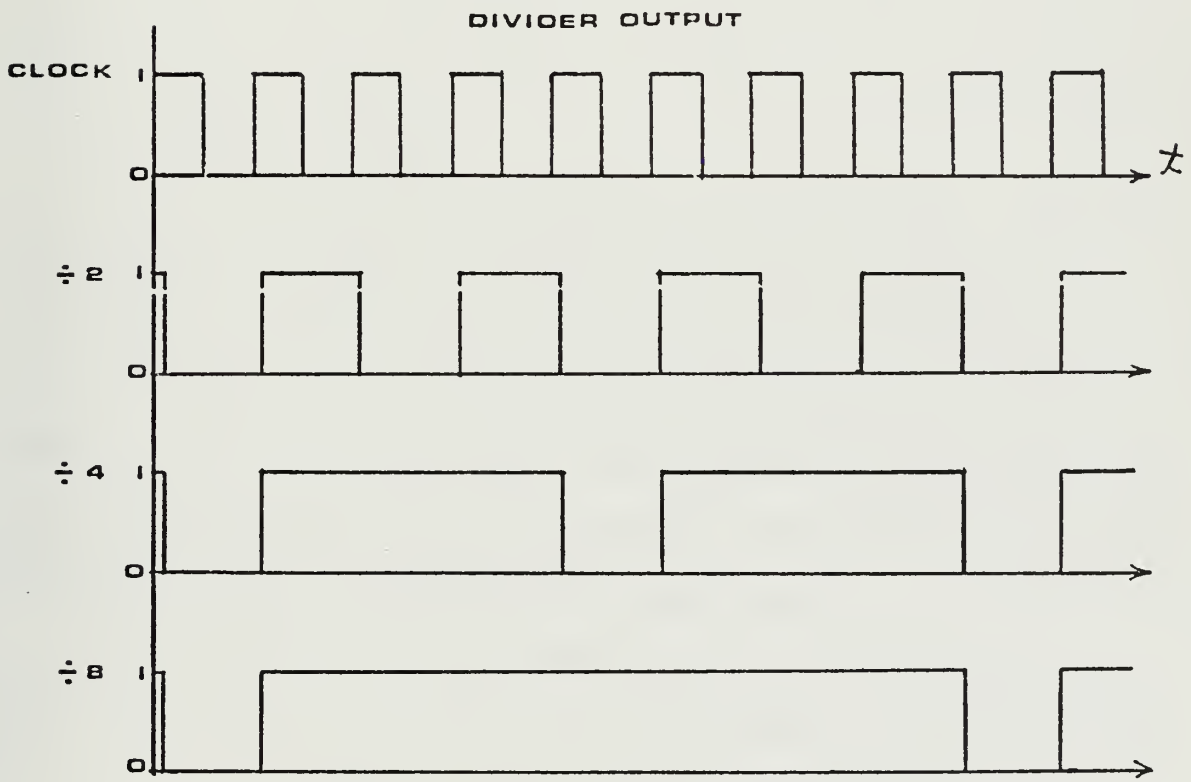


FIGURE 6

C. DELAY

The block diagram for the delay circuit is Figure 7. Following the CLEAR (CL) pulse both 8421 BCD (binary coded decimal) counters indicate zero and the 9020 FF has Q = 0, $\overline{Q}$ = 1. $\overline{Q}$ is ANDed with the 0.5 MHz pulse train which commences with the radar sync pulse. Because the output of the one in 10 decoder (Fairchild 9301) is zero it is necessary to AND this output with the Q output of the radar sync FF to decode zero at the proper time. At the tenth clock pulse the "9" makes the transition to the high state and this level is ANDed with the clock line to provide one count to the more significant decade at the next clock pulse. When both counters reach the pre-set switch position count the flip-flop toggles. $\overline{Q}$, now low, prevents further counting. Q is high and serves two purposes. First it performs the same type of "0 AND" function for the range gate counters and second it is ANDed with the basic clock line to permit counters to function.

The 8421 BCD counter was designed using JK flip-flops. The truth table and Veitch diagrams for minimization are shown in Appendix A. The output of the 8421 BCD counter applied to a Fairchild 9301 one-in-ten decoder provides low-level logic which necessitates inverting the output to obtain a positive pulse. One fourth of a Fairchild 9002 quad dual input NAND gate was used for inverting. This device was also used in constructing all of the AND gates in the circuit.

It was found that the delay time through the various circuits was short enough that the clock pulse was still present at the AND gate for the second stage when the "9" level arrived, resulting in one extra toggle. This problem was corrected by using the non-inverted "9". On the tenth clock pulse the "9" makes a transition from the low state to the high state which is the correct polarity for triggering the second

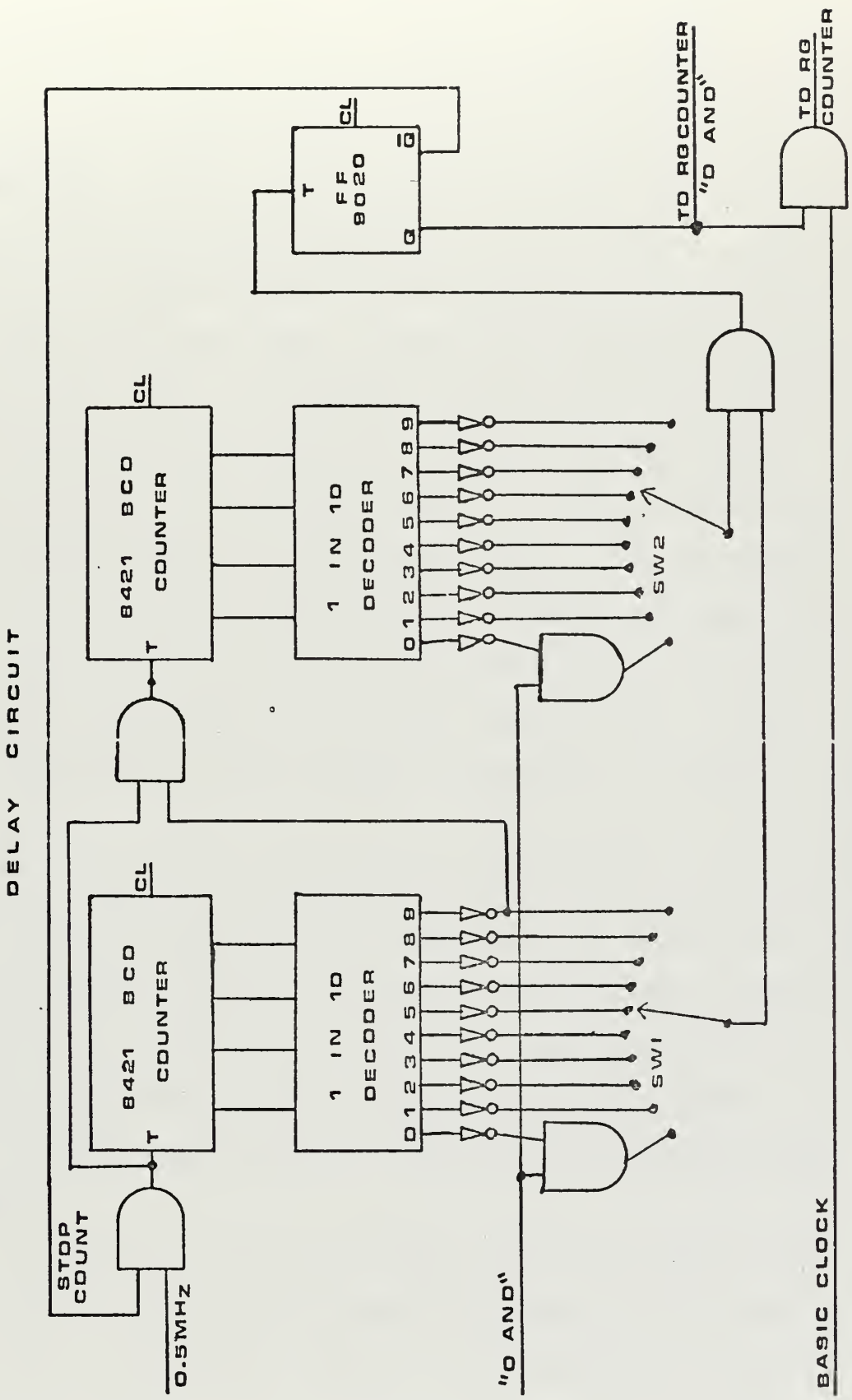

DELAY CIRCUIT
CL
FF
8020
T
Q
TO RG COUNTER
"0 AND"
TO RG COUNTER
CL
8421 BCD COUNTER
T
1 IN 10 DECODER
0 1 2 3 4 5 6 7 8 9
SW2
CL
8421 BCD COUNTER
T
1 IN 10 DECODER
0 1 2 3 4 5 6 7 8 9
SW1
STOP COUNT
0.5MHz
"0 AND"
BASIC CLOCK

FIGURE 7

stage. This version of the delay circuit counter is as indicated for the corresponding part of the gating circuit counter as shown in Figure 8.

D. RANGE GATES

The block diagram for the range-gate section is Figure 8. Upon completion of the delay time the final flip-flop in the delay circuit toggles which enables the "0 AND" and starts the train of clock pulses to counter number one. With the "0 AND" high the zeros of both decoders appear as high levels at the input to the RG number one NAND gate, causing it to go low. This provides a pulse of proper polarity to the sample-and-hold circuit of the first range channel. With the arrival of the first clock pulse to counter number one, range gate number two makes a transition to the low level and RG number one returns high, having been in the low state for the proper length of time. As the counter progresses this action continues through all of the range channels.

The first design utilized the same 8421 BCD counter as in the delay circuit. The whole circuit was very intolerant as far as the basic clock pulse was concerned at 4 MHz. It was found that the pulse amplitude had to be greater than 1.7 volts but less than 2.0 volts, and the pulse width less than 100 nsec for the ÷ 8 and ÷ 4 positions to operate properly. The 9301 decoded inverters were again constructed from 9002 NAND gates.

As one of the objectives was to reduce the size and weight of the system, it was decided to evaluate the Fairchild 9301 decade counter as a replacement for the 8421 BCD counter. This constitutes a savings of six integrated circuits. If the circuit is expanded to make use of all

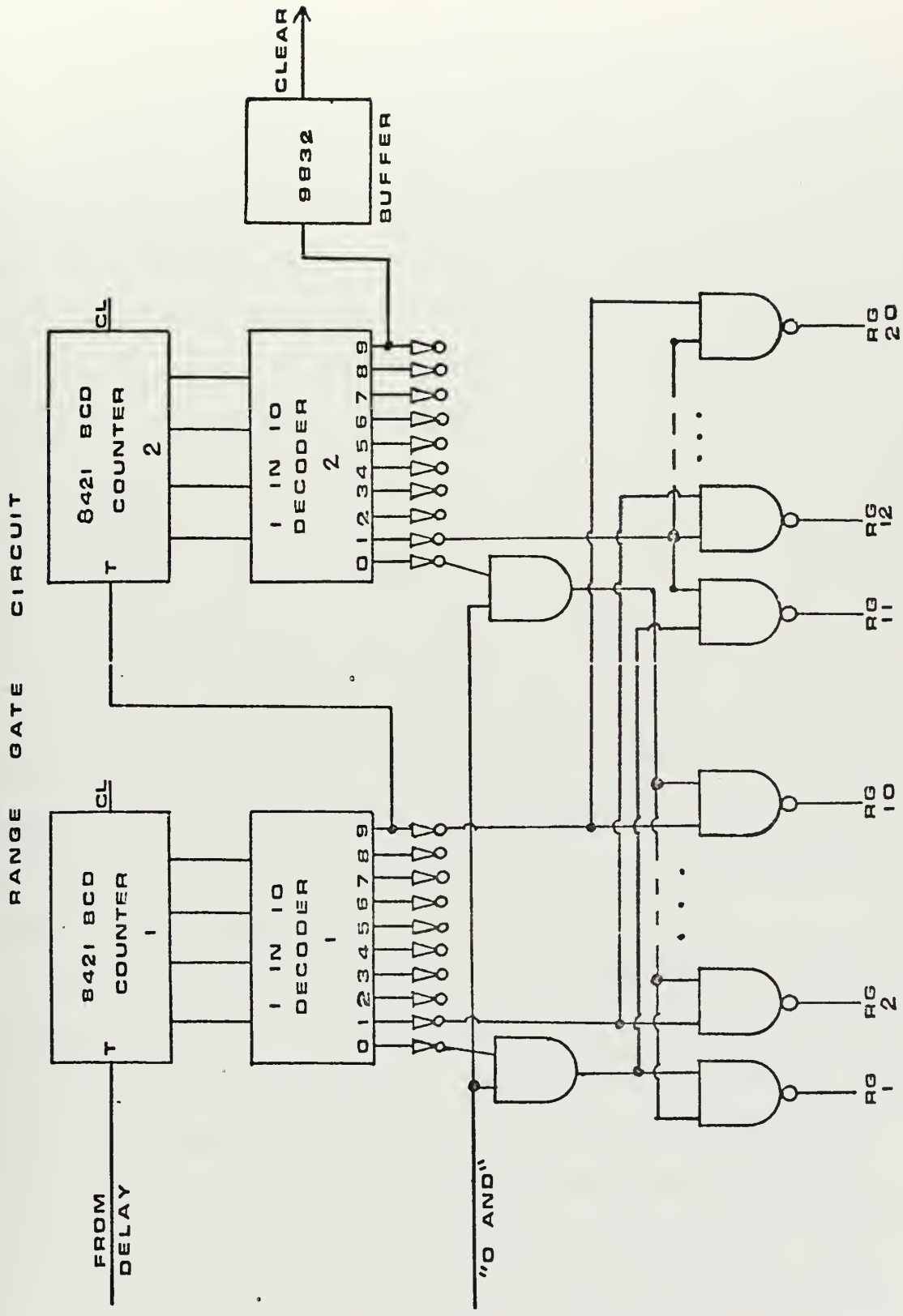

RANGE GATE CIRCUIT
CLEAR
9832
BUFFER
CL
8421 BCD COUNTER 2
T
1 IN 10 DECODER 2
0 1 2 3 4 5 6 7 8 9
CL
8421 BCD COUNTER 1
T
1 IN 10 DECODER 1
0 1 2 3 4 5 6 7 8 9
FROM DELAY
"0 AND"
RG 20
RG 12
RG 11
RG 10
RG 2
RG 1

FIGURE 8

available range channels each of the inverters will be required to fan-out to ten inputs; the maximum guaranteed fan-out capability of the device. It was decided to use the Fairchild 9932 four input NAND Buffers as an inverter for a margin of safety. This proved to be a superior arrangement from several standpoints. As mentioned above the number of devices was reduced by six. The device is almost noise free and the clock pulse tolerance was improved. The arrangement for triggering the second stage, indicated in Ref. 9 , made it unnecessary to use decoded outputs for this purpose and ensured the count on the correct pulse.

E. EXTENDABILITY

Extendability has been provided in design and in printed circuit board layout. Both the ÷ 4 and ÷ 8 can be changed to ÷ n, n = 2, 3, ...15, with a simple change to the input configuration of the 9300. Individual counters of the delay circuit are on separate boards. By providing one additional board which contains a third significant decade and another switch, delays up the full repetition period of the AN/UPS-1 radar could be obtained. The switches would have to be terminated by a three input AND (9003) rather than the 9002.

Each counter, with its decoder and associated inverters of the range-gate circuit, is on a separate board. With the present configuration ninety channels are available. It should be noted, however, that in the initial design the CLEAR pulse was formed on the twenty-first clock pulse. Race problems were encountered that were never fully understood in that periodically only twenty clock pulses were needed to CLEAR. These difficulties were removed by the use of the 9310 counters.

The addition of one counter in series will provide up to 900 channels (999 if the CLEAR is taken and the ANDing of all three "9's" before inverting).

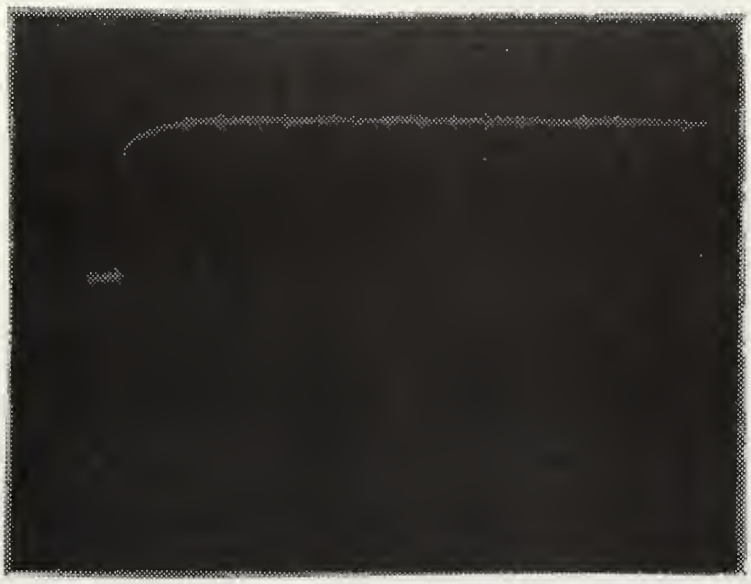
The outputs of the counters were NANDed in a 9932. Because of constraints imposed by the rack holding the printed circuit boards, there are but five NAND gates per board. The 9932 is a four input device which will facilitate extending the number of range channels beyond 99 by utilizing one of the unused inputs for the output of the additional counter stage.

The printed circuit board diagrams are included in Appendix B as an aid to future extension.

IV. RESULTS

The basic clock and the 800 Hz pulse train which in system testing simulated the radar trigger pulse train were supplied by separate Data Pulse Number 101 pulse generators. Provision was made on the circuit board containing the dividing circuitry for the inclusion of a crystal controlled oscillator similar to that found on page 111 of Ref. 10 when the optimum clock rate has been determined.

Upon testing the dividing circuitry a disadvantage of the system was discovered. When the first flip-flop makes the transition to the high state as a result of the radar pulse the divider output may just have gone low. Thus as many as seven additional clock pulses were possible before the first count was recorded in the delay circuitry with the switch in the ÷ 8 position. This introduced a jitter into the delay which is a function of clock rate and switch position. An analysis of this effect is included as Appendix C. Jitter on either side of the desired delay greater than one range gate width would result in overlapping of range channels from pulse to pulse. This is true of the ÷ 4 and ÷ 8 positions at all frequencies. The final solution to the problem is to synchronize the radar to the clock, thus eliminating jitter entirely. Figure 9 depicts a typical gate pulse. In the upper photograph the oscilloscope has been synchronized internally to show a single pulse. In the lower photograph the oscilloscope has been synchronized to the 800 Hz pulse train so that delay and jitter can be observed.



Verticle Scale: 2 V/div
Horizontal Scale: 2 μsec/div

Verticle Scale: 2 V/div
Horizontal Scale: 2 μsec/div

Figure 9. Gating Pulse.

The 8421 BCD counters constructed from J-K flip-flops were found to be very noisy. This noise manifested itself in the form of spurious responses appearing in the output of the decoders. As suggested in Ref. 11 the problems from these spurious responses were eliminated by placing a small capacitor to ground at any noisy output of the decoders. As mentioned in a previous section the 9310 counters were almost noise free, and no capacitor filtering was required.

For evaluation, each of the twenth channels was used to gate the sample-and-hold circuit of a range channel designed by D. B. Hoisington, Figure 10.

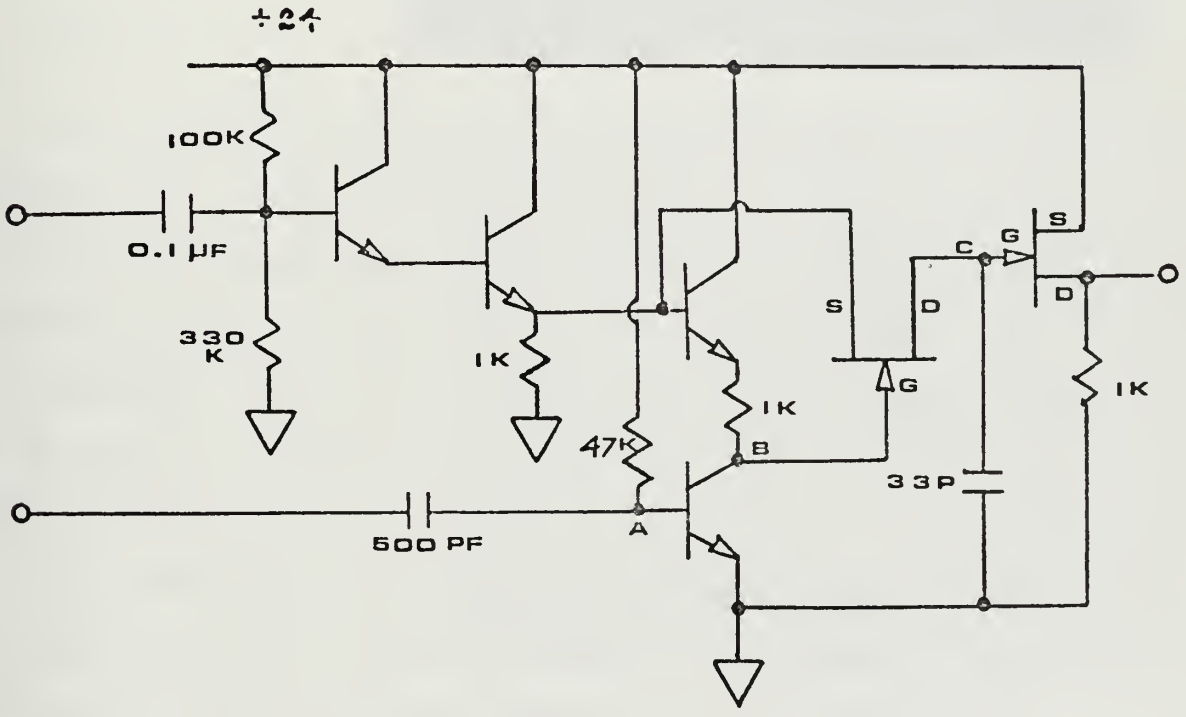


FIGURE 10

The performance of each of the channels was identical so that the following discussion applies to all. A sine wave of about 100 Hz was used to represent the bipolar video of the radar. The sampling frequency was 1.0 MHz and the divider switch was in the ÷ 2 position. Therefore the output of each channel of the timing and gating circuitry was a 800

Hz train of 1.0 usec pulses. The top trace of Figure 11 shows the pulse train at point A of Figure 10. The bottom trace is at point B.

Sample and Hold

Top trace
Verticle Scale:
2V/div.
Horizontal Scale:
2 μsec/div.

Bottom Trace
Verticle Scale:
10V/div.
Horizontal Scale:
2 μsec/div.

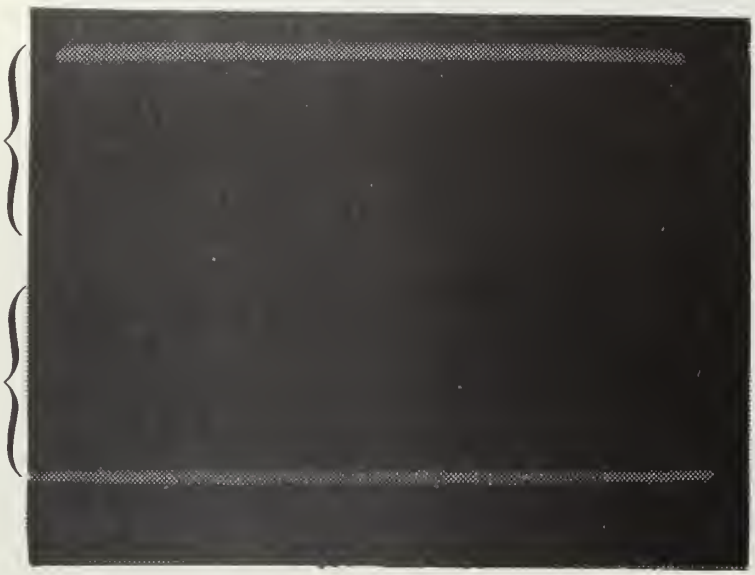


Figure 11

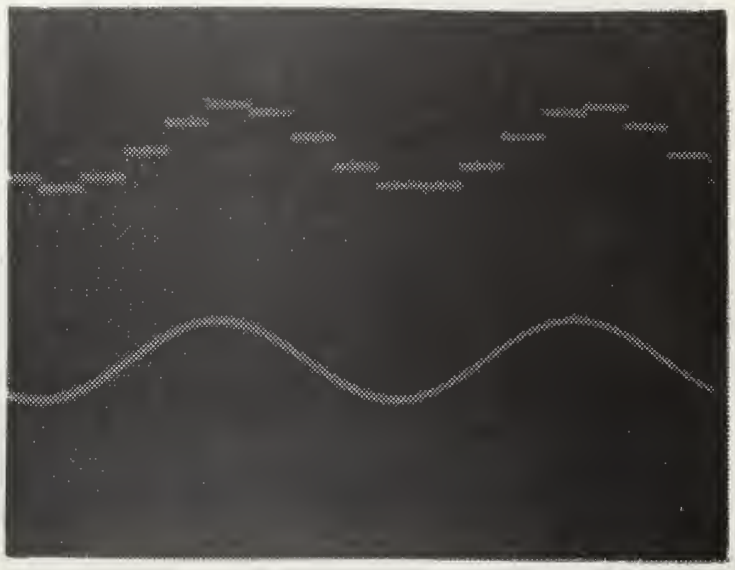
In Figure 12 the signal wave form is the lower trace of the upper photograph. The samples taken appear as the lower trace in the lower photograph. This sample having been stretched by the holding circuitry appeared at point C as in the upper trace of both photographs. The final photograph, Figure 13, shows the input waveform in the upper trace and the output of a typical pass-band filter following the sample and hold in the lower trace.

It was noted that if the frequency of the input signal was reduced the output went to zero. When the frequency was increased null points were observed at the first few multiples of the pulse repetition frequency such that a close approximation to the ideal filter of Figure 2 had been obtained. A further increase in signal frequency beyond about 100 kHz did not produce the desired results. This was attributed to the jitter in the delay time.

Sample and Hold

Verticle Scale:
10V/div.

Horizontal Scale:
2 μsec/div.



Verticle Scale:
10V/div.

Horizontal Scale:
2 μsec/div.

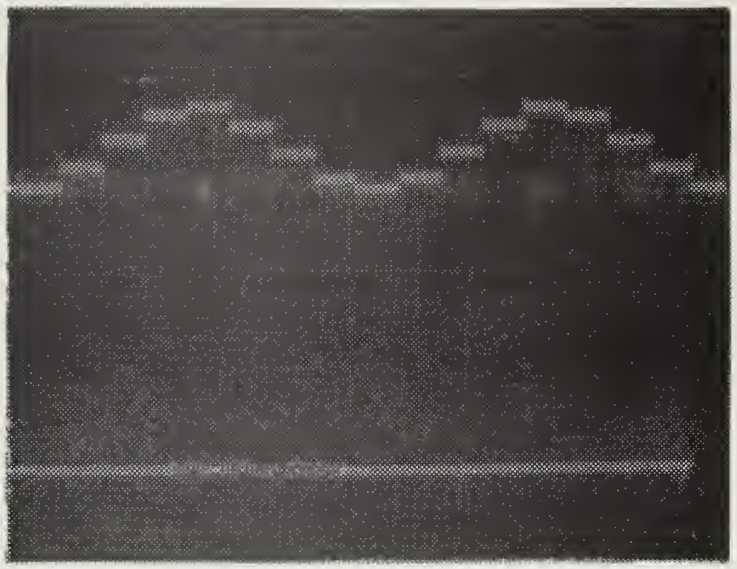


Figure 12.

Signal

Verticle Scale:
5V/div.

Horizontal Scale:
5 μsec/div.

Filter Output

Verticle Scale:
5V/div.

Horizontal Scale:
5 μsec/div.

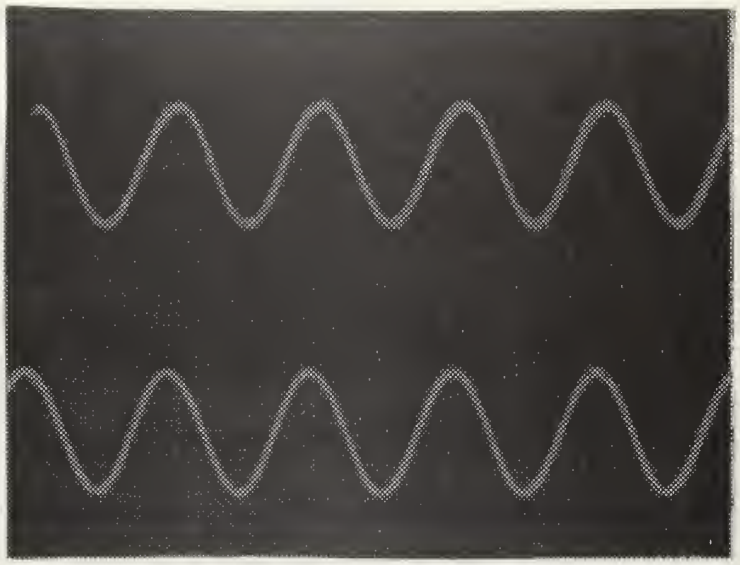


Figure 13

V. SUMMARY AND CONCLUSIONS

Timing circuitry was constructed which provides for twenty channels of range-gated MTI radar. It is possible through delay circuitry, to vary the range interval at which the twenty gates operate from zero to about sixteen nautical miles. This feature will be useful in minimizing the number of channels required in evaluating operation of this system to an extended range. The use of integrated circuits made it possible to design for flexibility and extendability while maintaining good economy.

The system is intended to be evaluated in conjunction with the AN/UPS-1 radar and in parallel with that radar's delay-line canceler. In this case it will be difficult to synchronize the radar with the master clock because the delay-line canceler must necessarily provide its own synchronization. In any synchronized system all parts of that system must be synchronized with the master clock; thus in the case where range gates are being compared in parallel with a delay-line canceler it will be necessary to have the sampling clock be a harmonic frequency of the pulse repetition rate or to be triggered by each successive synchronizing pulse.

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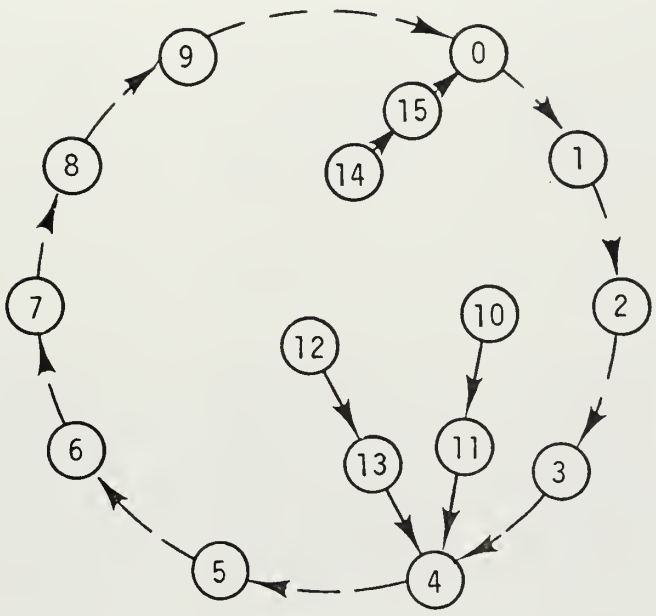
APPENDIX A: 8421 BCD COUNTER

An 8421 BCD counter is a four-bit binary counter in which the most significant bit is equal to $2^3 = 8$; the next equal to $2^2 = 4$ and so forth. The count progresses from $0000_2 = 0_{10}$ to $1001_2 = 9_{10}$ and then returns to 0_{10}, thus it is a binary-coded-decimal counter. The counter can be realized with four clocked flip-flops, W, X, Y and Z, having appropriate logical interconnections. The attached truth table indicates the transition from one state to the next for all combinations of four-bit numbers.

Because the possibility exists for the counter to get into a state other than 0_{10} - 9_{10}, those states must return to the desired counting sequence for proper operation. These illegal state transitions are also indicated in the truth table. The entire counting sequence is depicted in the state diagram.

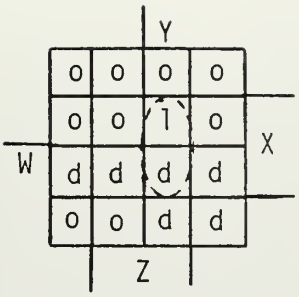
The truth table represents a Boolean expression which can take many forms. These are several methods by which this expression can be minimized as indicated by Chu [Ref. 13] and minimization of a Boolean expression usually results in minimization of hardware. In this case minimization by the Veitch diagram was chosen for realization with JK flip-flops. Because of the logical input configuration of the Fairchild 9020 dual JK flip-flop, it was necessary to use three of those integrated circuits to build the counter.

STATE DIAGRAM

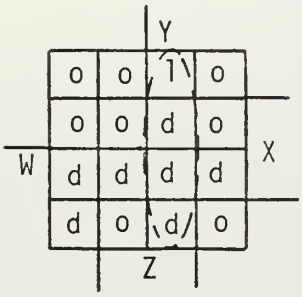


VEITCH MINIMIZATION

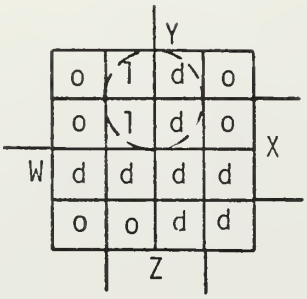
CLOCKED JK FF



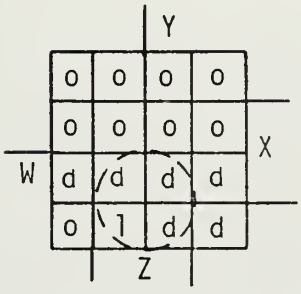
$J_W = XYZ$



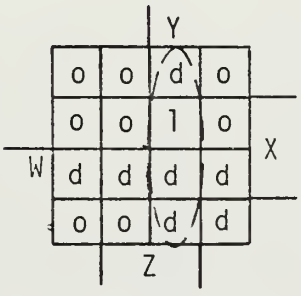
$J_X = YZ$



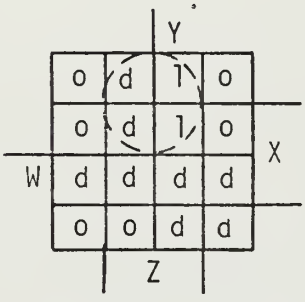
$J_y = WZ$ $J_z = 1$



$K_W = WZ$



$K_X = YZ$



$K_y = WZ$ $K_z = 1$

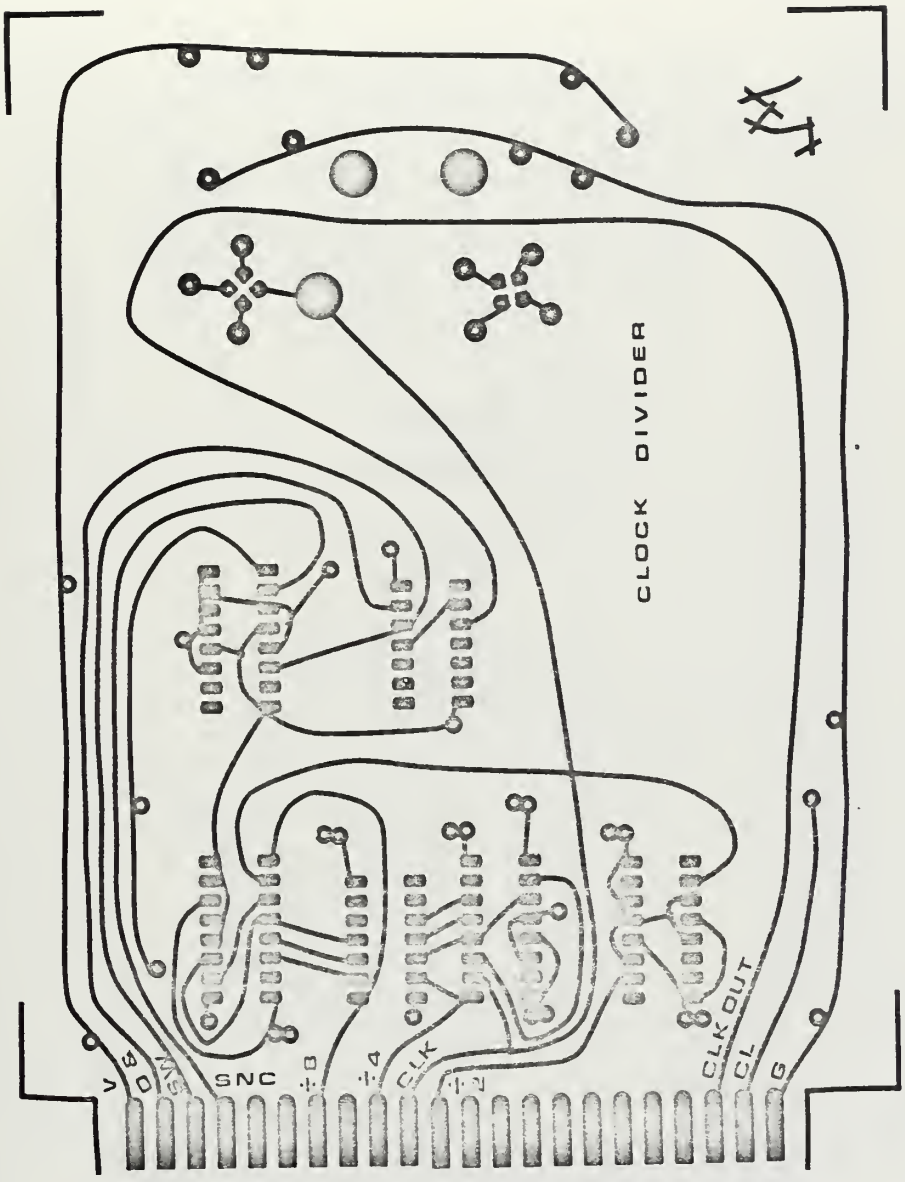
8421 BCD COUNTER TRUTH TABLE

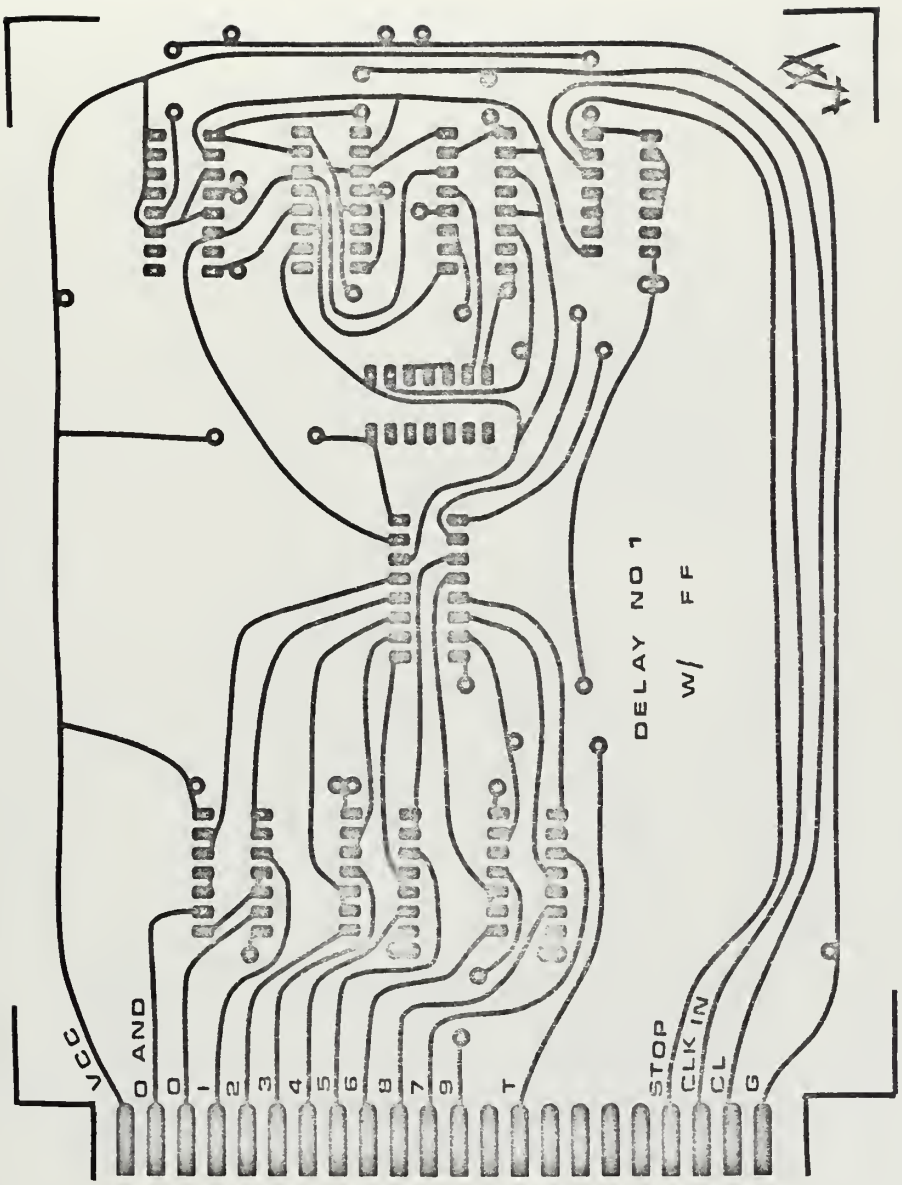
	PRESENT STATE				NEXT STATE				
	w	x	y	z	W	X	Y	Z	
0	0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	0	1	0	2
2	0	0	1	0	0	0	1	1	3
3	0	0	1	1	0	1	0	0	4
4	0	1	0	0	0	1	0	1	5
5	0	1	0	1	0	1	1	0	6
6	0	1	1	0	0	1	1	1	7
7	0	1	1	1	1	0	0	0	8
8	1	0	0	0	1	0	0	1	9
9	1	0	0	1	0	0	0	0	0
10	1	0	1	0	1	0	1	1	11
11	1	0	1	1	0	1	0	0	4
12	1	1	0	0	1	1	0	1	13
13	1	1	0	1	0	1	0	0	4
14	1	1	1	0	1	1	1	1	15
15	1	1	1	1	0	0	0	0	0

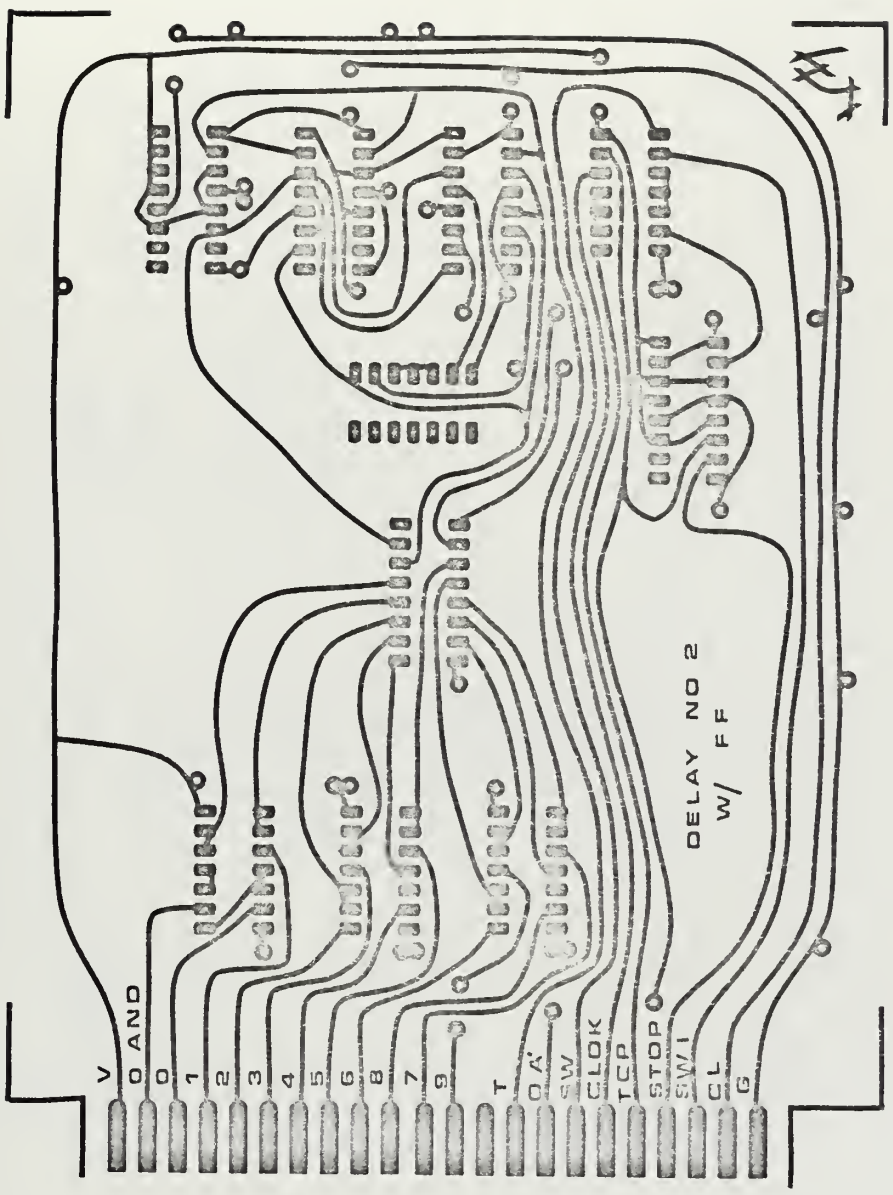
ILLEGAL STATES

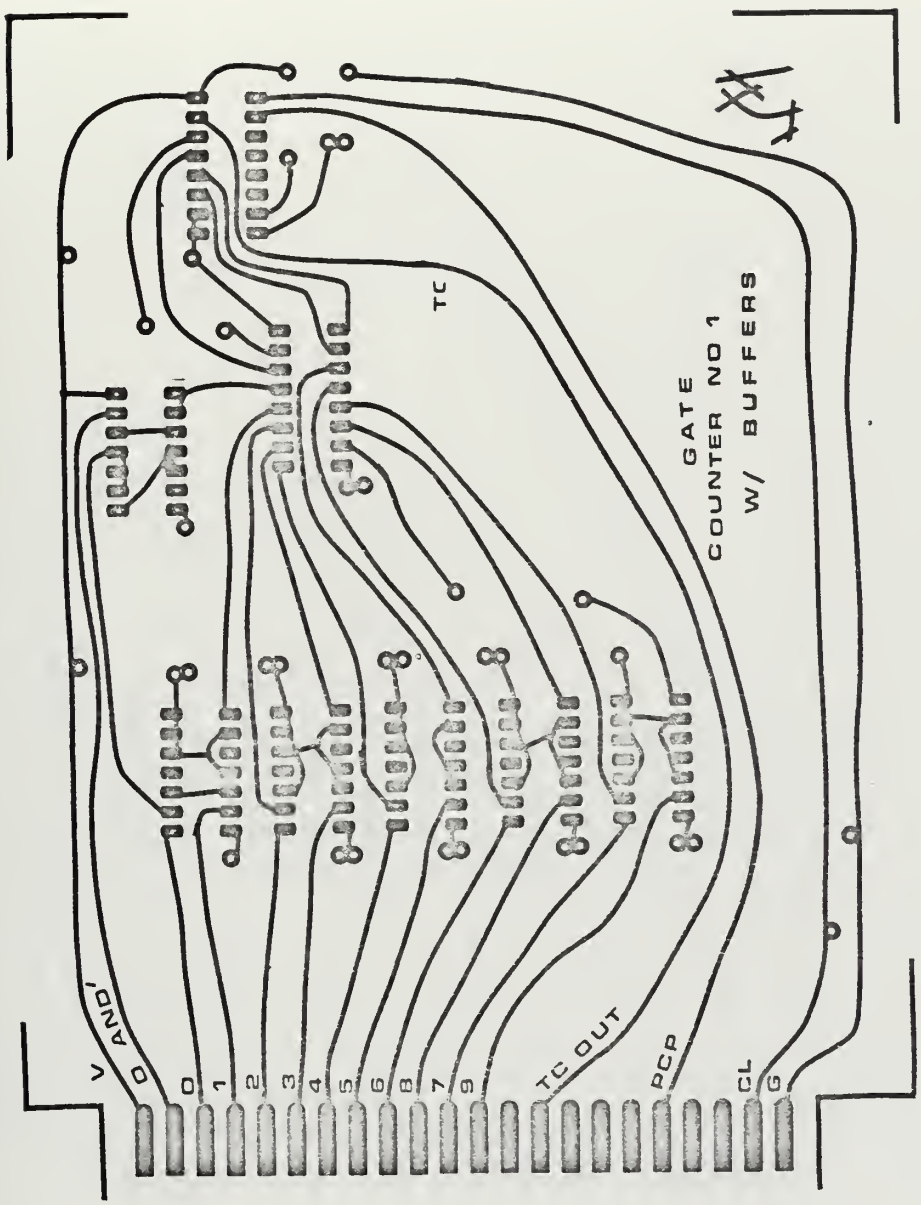
APPENDIX B: PRINTED CIRCUIT DIAGRAMS

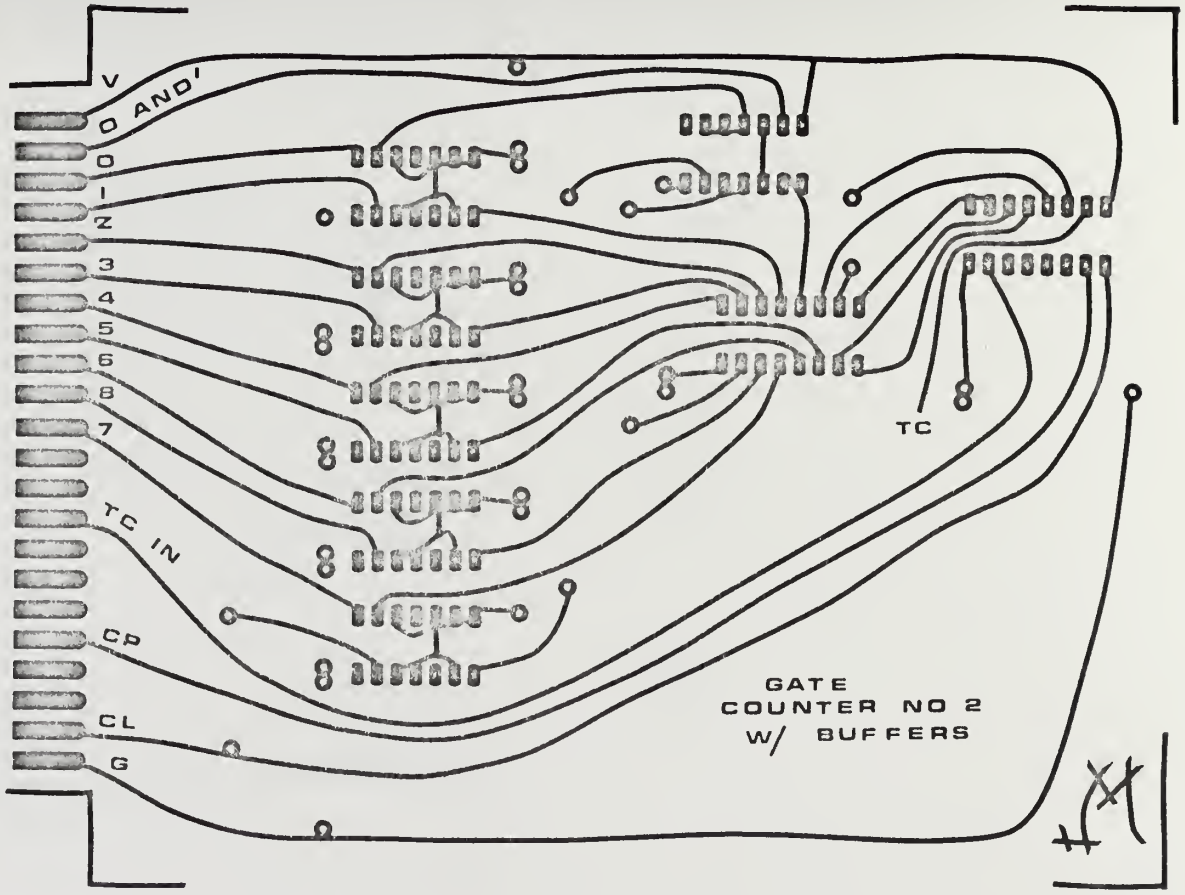
The following diagrams show the foil side of the printed circuit boards and represent how each board is presently configured electrically. Because of changes made during construction and testing some boards have jumper wires on them which have been replaced by foil connections in these diagrams.


CLOCK DIVIDER
VSS
SNC
÷8
÷4
CLK
÷2
CLK OUT
CL
G


VCC
0 AND
0
1
2
3
4
5
6
8
7
9
T
STOP
CLK IN
CL
G
DELAY NO 1
W/ FF

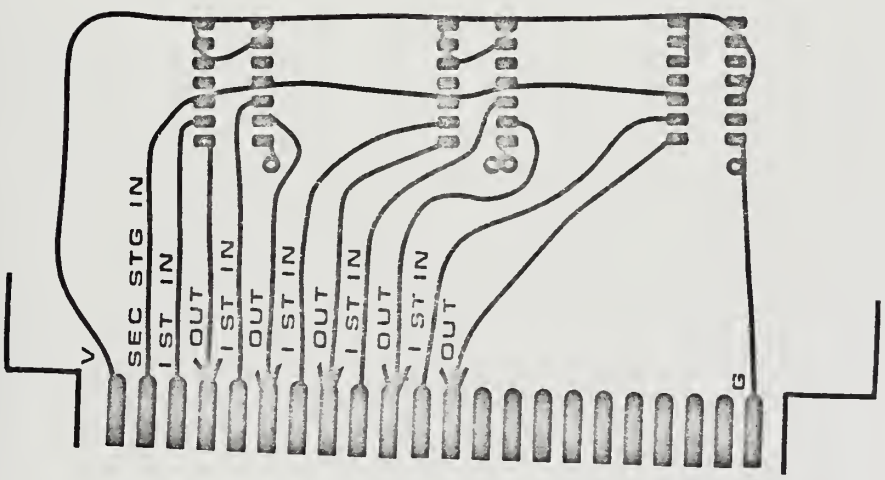

V
0 AND
0
1
2
3
4
5
6
8
7
9
T
0A
SW
CLOK
TCP
STOP
SW1
CL
G
DELAY NO 2
W/ FF


GATE
COUNTER NO 1
W/ BUFFERS
TC
V AND' D
0
1
2
3
4
5
6
8
7
9
TC OUT
PCP
CL
G


V
0 AND'
0
1
2
3
4
5
6
8
7
TC IN
CP
CL
G
TC
GATE
COUNTER NO 2
W/ BUFFERS

NANDING BOARDS

USING 9932



APPENDIX C: JITTER EVALUATION

The amount of jitter listed in the attached table represents the average of the first ten channels as obtained with clock pulses synchronized by the sync pulses of the simulated radar. The data was taken at each clock rate and at each division setting with delays of 4.0, 20.0, and 40.0 usec. Because of drift in the frequency of the clock, the pulse width was checked and adjusted if necessary before each measurement.

Clock Rate	Pulse Width	Divide by	Jitter
4 MHz	0.25 usec	8	2 usec
	0.25 usec	4	1 usec
	0.25 usec	2	0.6 usec
	0.25 usec	1	0.4 usec
2 MHz	0.5 usec	8	4.0 usec
	0.5 usec	4	2.3 usec
	0.5 usec	2	1.3 usec
	0.5 usec	1	0.8 usec
1 MHz	1.0 usec	8	8.5 usec
	1.0 usec	4	4.8 usec
	1.0 usec	2	2.6 usec
	1.0 usec	1	1.6 usec
0.5 MHz	2.0 usec	8	16.0 usec
	2.0 usec	4	9.4 usec
	2.0 usec	2	5.6 usec
	2.0	1	3.8 usec

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DOCUMENT CONTROL DATA - R & D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1 ORIGINATING ACTIVITY (Corporate author)

Naval Postgraduate School
Monterey, California 93940

2a. REPORT SECURITY CLASSIFICATION

Unclassified

2b. GROUP

3 REPORT TITLE

Controlling of Range-Gated MTI Radar With Digital Techniques

4 DESCRIPTIVE NOTES (Type of report and inclusive dates)

Master's Thesis; June 1971

5. AUTHOR(S) (First name, middle initial, last name)

John Warren Millard

6. REPORT DATE	7a. TOTAL NO. OF PAGES	7b. NO. OF REFS
June 1971	48	12

8a. CONTRACT OR GRANT NO.	9a. ORIGINATOR'S REPORT NUMBER(S)
b. PROJECT NO.	
c.	9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report)
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13. ABSTRACT

The timing and gating circuitry necessary for twenty channels of range-gated MTI radar was constructed. By the incorporation of a variable delay in the commencement of the range-gate sampling interval it was possible to extend the effective range over which the gates operated. The use of digital techniques with integrated circuits provided a means by which the twenty channels may easily be extended to any number required for a particular radar application. Performance of the circuitry was demonstrated in conjunction with a typical channel of range-gated MTI radar.

DD FORM 1 NOV 65 1473 (PAGE 1)

S/N 0101-807-6811

A-31408

KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Radar						
Moving Target Indicator						
Digital Control						

Thesis
M5853 Millard
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Controlling of range-gated MTI radar with digital techniques.